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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,223	01/22/2004	Hiroyuki Fukunaga	OKI.616	2739
20987	7590	05/17/2006	EXAMINER KEBEDE, BROOK	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/761,223

Applicant(s)

FUKUNAGA, HIROYUKI

Examiner

Brook Kebede

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on 07 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 5-14 is/are pending in the application.
- 4a) Of the above claim(s) 2,7,8 and 12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,5,6,9-11,13 and 14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 8/5/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Species I, i.e., Claims 1, 5, 6, and 11 in the reply filed on March 7, 2006 is acknowledged. In addition, applicants contend that claims 9, 10, 13 and 14 are also generic.
2. Accordingly, claims 2, 7, 8 and 12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on March 7, 2006

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 5, 6, 9-11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al. (US/4,514,897) in view of Fujii et al. (US/5,017,979).

Re claim 1, Chiu et al. disclose A method of manufacturing a nonvolatile semiconductor storage device, comprising: the first step of successively forming a first insulating film (23) and a first polysilicon layer (13) on a semiconductor substrate (20); patterning the first polysilicon layer (13) and the first insulating (23) film into the shape of a band; thermally oxidizing the patterned band-shaped first polysilicon layer (13), thereby to form a second insulating film (24) which is thicker at side surfaces of the first polysilicon layer (13) than at the front surface thereof; forming a second polysilicon layer (14) on a front surface of the resulting semiconductor

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substrate formed with the second insulating film (24); performing patterning so as to form each storage element of the nonvolatile semiconductor storage device as includes the first insulating film (23), a floating gate electrode made of the first polysilicon layer (13), the second insulating film (24), and a control gate electrode made of the second polysilicon layer (14) (see Figs. 2, 5a-5f, and 7 and related text in Col. 2, line 40 – Col. 8, line 15).

However, Chiu et al. do not specifically disclose implanting nitrogen ions into a front surface of the first polysilicon layer.

Fujii et al. disclose a method of fabricating nonvolatile memory device the method includes firing the first polysilicon layer (42) on the first simulating layer (40) and implanting of the first polysilicon layer with nitrogen ion in order to form a barrier layer that blocks impurities from the polysilicon layer (see Fujii et al. Fig. 14A and Col. 10, lines 18-27).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Chiu et al. reference with implanting nitrogen ions into a front surface of the first polysilicon layer as taught by Fujii et al. order to form a barrier layer that blocks impurities from the polysilicon layer.

Re claim 5, as applied to claim 1 above, Chiu et al. and Fujii et al. in combination disclose all the claimed limitations including wherein the nitrogen ions are implanted into the first polysilicon layer so as to be located only in the front surface of the first polysilicon layer (see Chiu et al. Figs. 2, 5a-5f, and 7 and related text in Col. 2, line 40 – Col. 8, line 15; and Fujii et al. Fig. 14A and Col. 10, lines 18-27).

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Re claim 6, as applied to claim 1 above, Chiu et al. and Fujii et al. in combination disclose all the claimed limitations including wherein the first polysilicon layer has a thickness of 20 – 40 nm (i.e., within the overlap claimed range of 20 to 50 nm) implanting nitrogen ions with predetermined energy and ion concentration. Furthermore, the claimed nitrogen dopant energy level and ion concentration can be achieved by routine optimization in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to the dopant energy and concentration level, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed acceleration voltage as well as dopant concentration or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claims 9-11, Chiu et al. disclose a method of manufacturing a nonvolatile semiconductor storage device, comprising: the first step of successively forming a first insulating film (23) and a first polysilicon layer (13) on a semiconductor substrate (20); patterning the first

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polysilicon layer (13) and the first insulating (23) film into the shape of a band; thermally oxidizing the patterned band-shaped first polysilicon layer (13), thereby to form a second insulating film (24) which is thicker at side surfaces of the first polysilicon layer (13) than at the front surface thereof; forming a second polysilicon layer (14) on a front surface of the resulting semiconductor substrate formed with the second insulating film (24); performing patterning so as to form each storage element of the nonvolatile semiconductor storage device as includes the first insulating film (23), a floating gate electrode made of the first polysilicon layer (13), the second insulating film (24), and a control gate electrode made of the second polysilicon layer (14) (see Figs. 2, 5a-5f, and 7 and related text in Col. 2, line 40 – Col. 8, line 15).

However, Chiu et al. do not specifically disclose implanting nitrogen ions into a front surface of the first polysilicon layer.

Fujii et al. disclose a method of fabricating nonvolatile memory device the method includes firming the first polysilicon layer (42) on the first simulating layer (40) and implanting of the first polysilicon layer with nitrogen ion in order to form a barrier layer that blocks impurities form the polysilicon layer (see Fujii et al. Fig. 14A and Col. 10, lines 18-27).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Chiu et al. reference with implanting nitrogen ions into a front surface of the first polysilicon layer as taught by Fujii et al. order to form a barrier layer that blocks impurities form the polysilicon layer.

Re claim 13, as applied to claim 9 above, Chiu et al. and Fujii et al. in combination disclose all the claimed limitations including wherein the nitrogen ions are implanted into the first polysilicon layer so as to be located only in the front surface of the first polysilicon layer

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(see Chiu et al. Figs. 2, 5a-5f, and 7 and related text in Col. 2, line 40 – Col. 8, line 15; and Fujii et al. Fig. 14A and Col. 10, lines 18-27).

Re claim 14, as applied to claim 9 above, Chiu et al. and Fujii et al. in combination disclose all the claimed limitations including wherein the first polysilicon layer has a thickness of 20 – 40 nm (i.e., within the overlap claimed range of 20 to 50 nm) implanting nitrogen ions with predetermined energy and ion concentration. Furthermore, the claimed nitrogen dopant energy level and ion concentration can be achieved by routine optimization in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to the dopant energy and concentration level, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed acceleration voltage as well as dopant concentration or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

***Response to Arguments***

5. Applicants' arguments with respect to claims 5, 6, 9-11, 13 and 14 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on August 5, 2005.

6. Applicant's arguments filed on August 5, 2005 with respect to claim 1 have been fully considered but they are not persuasive.

Applicant argues that "Chiu et al. reference does not disclose silicon layer 24 formed so as thicker on the side surfaces of floating gate 13 than the front surface ..."

In response to applicant's argument, it is respectfully submitted the combination of Chiu et al. '897 and Fujii et al. '979 disclose all the claimed limitations claim 1 as applied in paragraph 4 above. As shown Fig. 2, the silicon oxide layer 24 appears thicker in bottom edge surface of the floating gate 13 than the top surface of floating gate 13. In addition, in the absence of specification thickness range of the silicon oxide layer on the top surface relative to the sidewall surface of the floating gate applicant's own drawings are not drawn to scale.

Claims are given claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.



***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

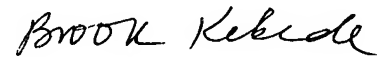
***Correspondence***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brook Kebede  
Primary Examiner  
Art Unit 2823

BK  
May 15, 2006